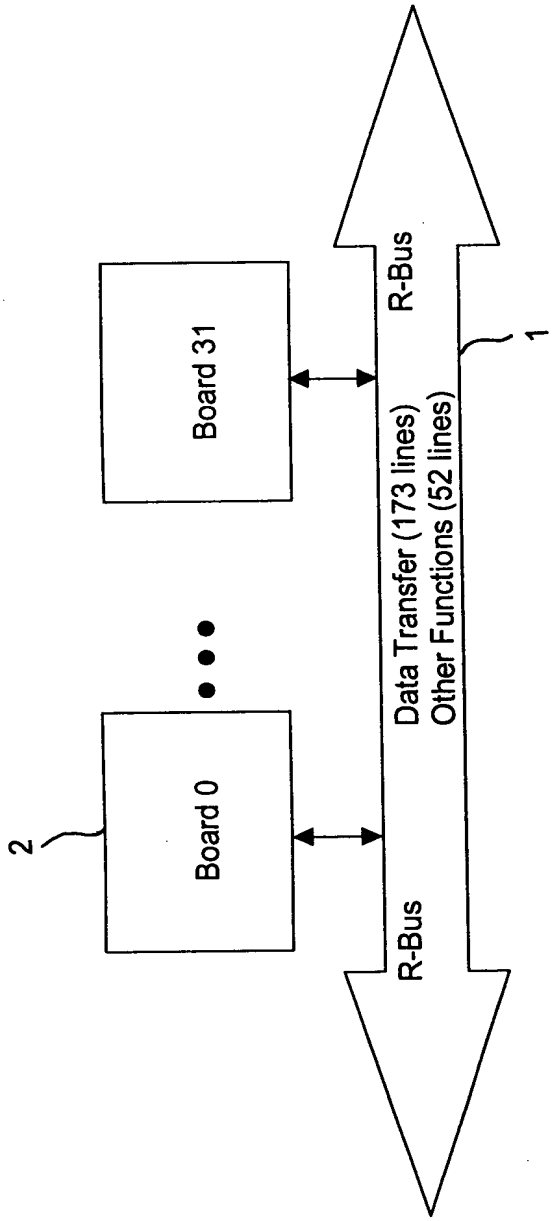
Board 31
Board 0
R-Bus
Data Transfer (173 lines)
Other Functions (52 lines)
R-Bus
1
2

FIG. 1

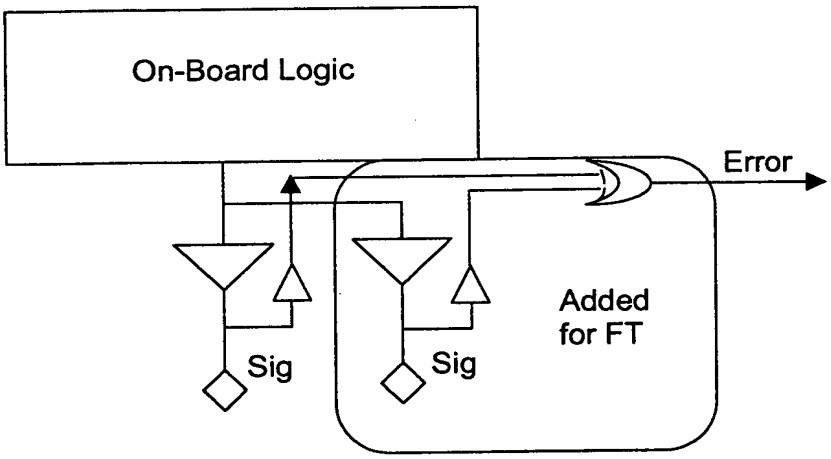

FIG. 2

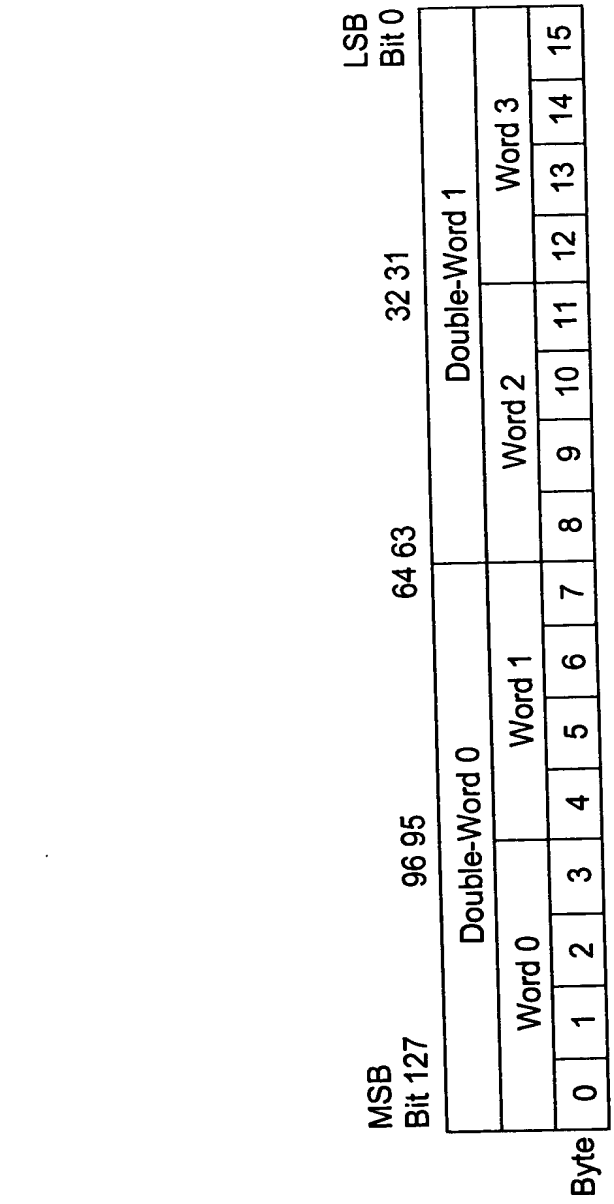
MSB
Bit 127
96 95
64 63
32 31
LSB
Bit 0
Double-Word 0
Double-Word 1
Word 0
Word 1
Word 2
Word 3
Byte
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

FIG. 3

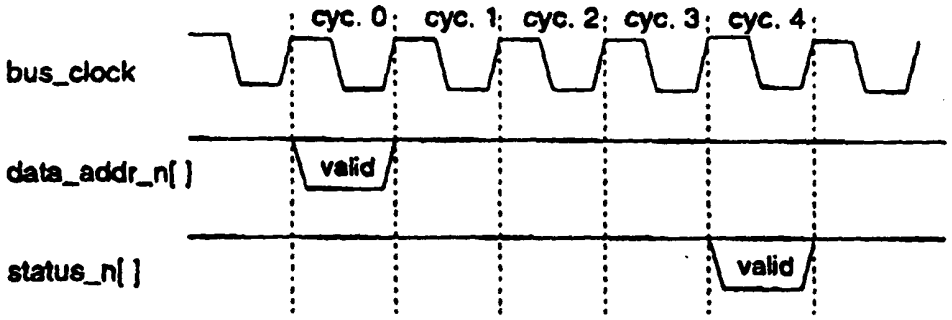
cyc. 0
cyc. 1
cyc. 2
cyc. 3
cyc. 4
bus_clock
data_addr_n[ ]
valid
status_n[ ]
valid

FIG. 4

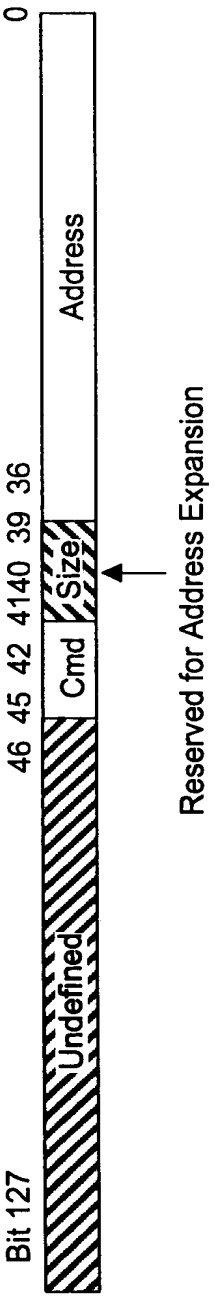
Bit 127
46
45
42
41
40
39
36
0
Undefined
Cmd
Size
Address
Reserved for Address Expansion

FIG. 5

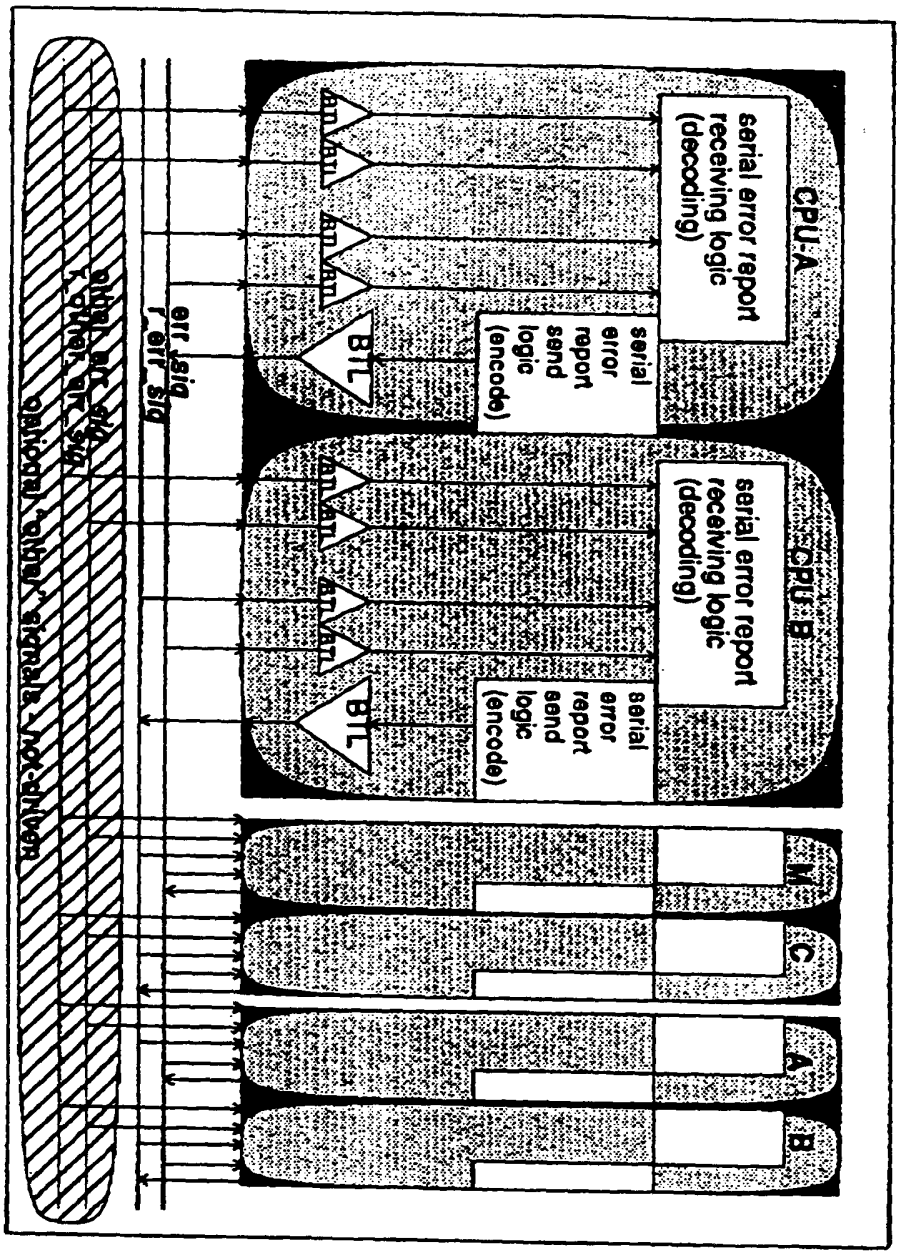
CPU A
serial error report receiving logic (decoding)
serial error report send logic (encode)
BTL
CPU B
serial error report receiving logic (decoding)
serial error report send logic (encode)
BTL
M
C
A
B
err_sig
r_err_sig

FIG. 6

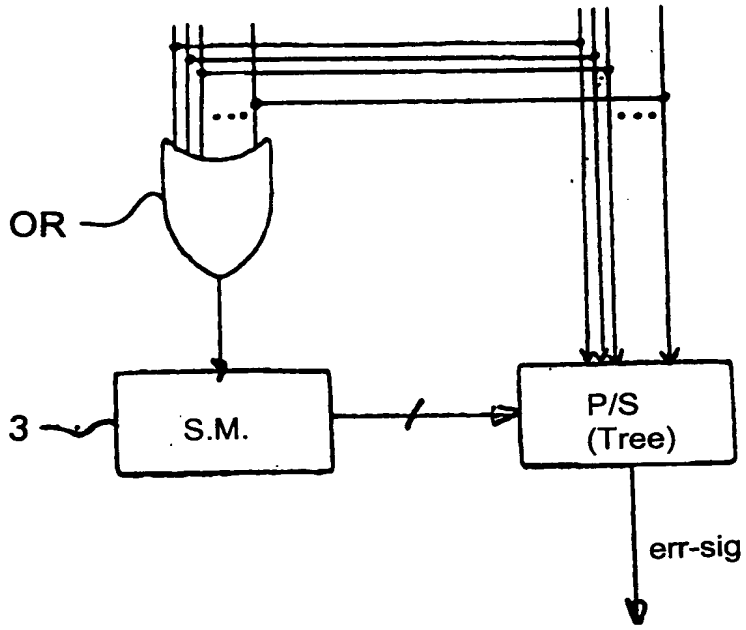
OR
3
S.M.
P/S
(Tree)
err-sig

FIG. 7

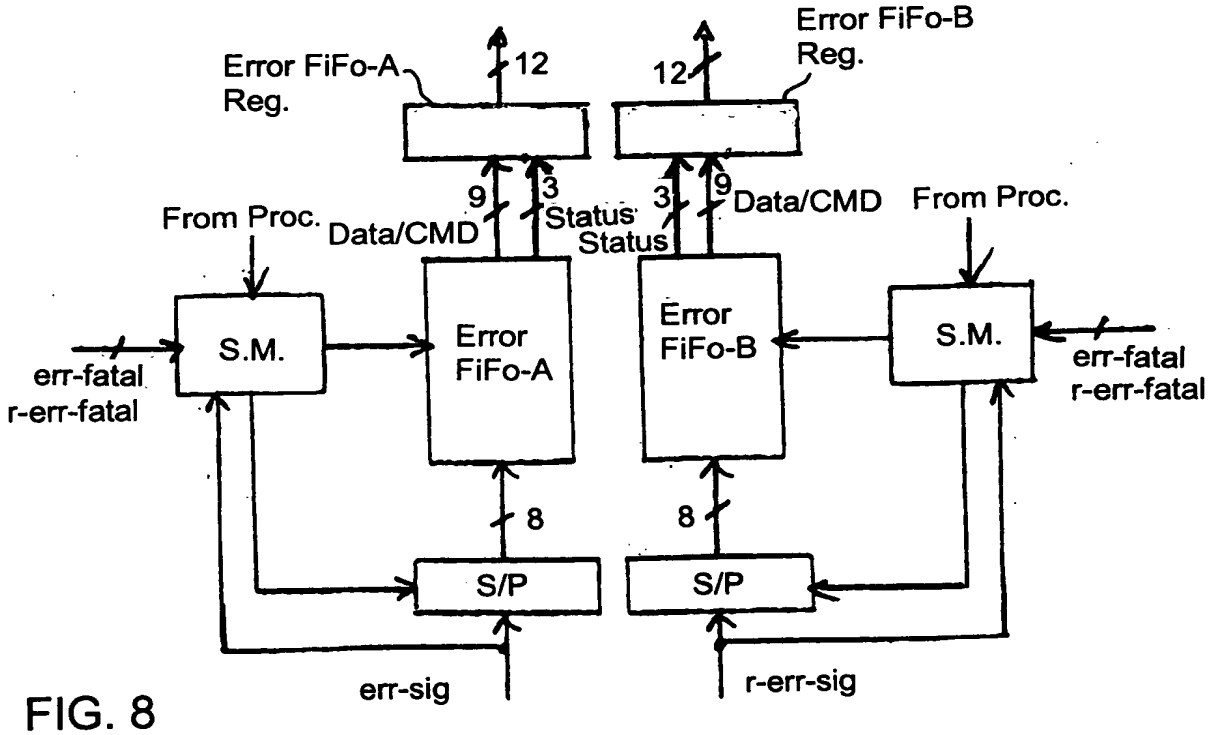
Error FiFo-A
Reg.
12
12
Error FiFo-B
Reg.
9
3
Status
3
9
Data/CMD
From Proc.
Data/CMD
Status
From Proc.
S.M.
Error
FiFo-A
Error
FiFo-B
S.M.
err-fatal
r-err-fatal
err-fatal
r-err-fatal
8
8
S/P
S/P
err-sig
r-err-sig

FIG. 8

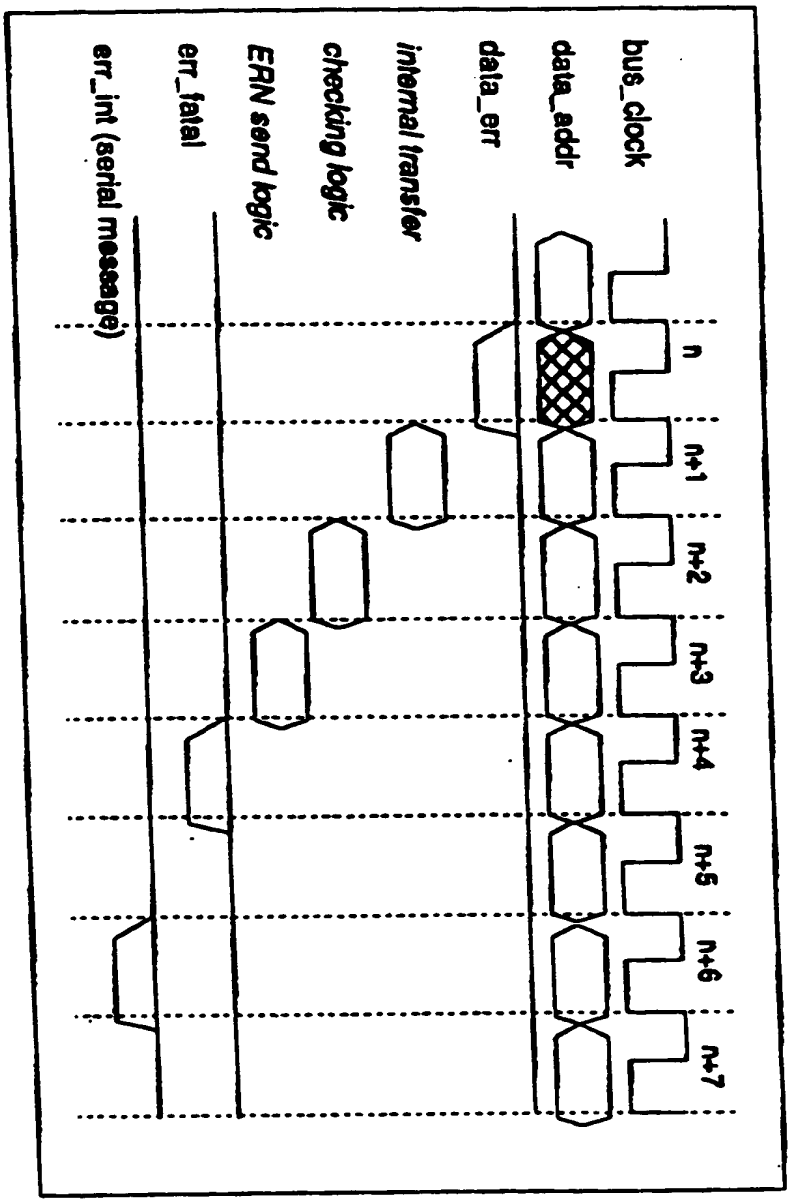
bus_clock
data_addr
data_err
internal transfer
checking logic
ERN send logic
err_fatal
err_int (serial message)
n
n+1
n+2
n+3
n+4
n+5
n+6
n+7

FIG. 9

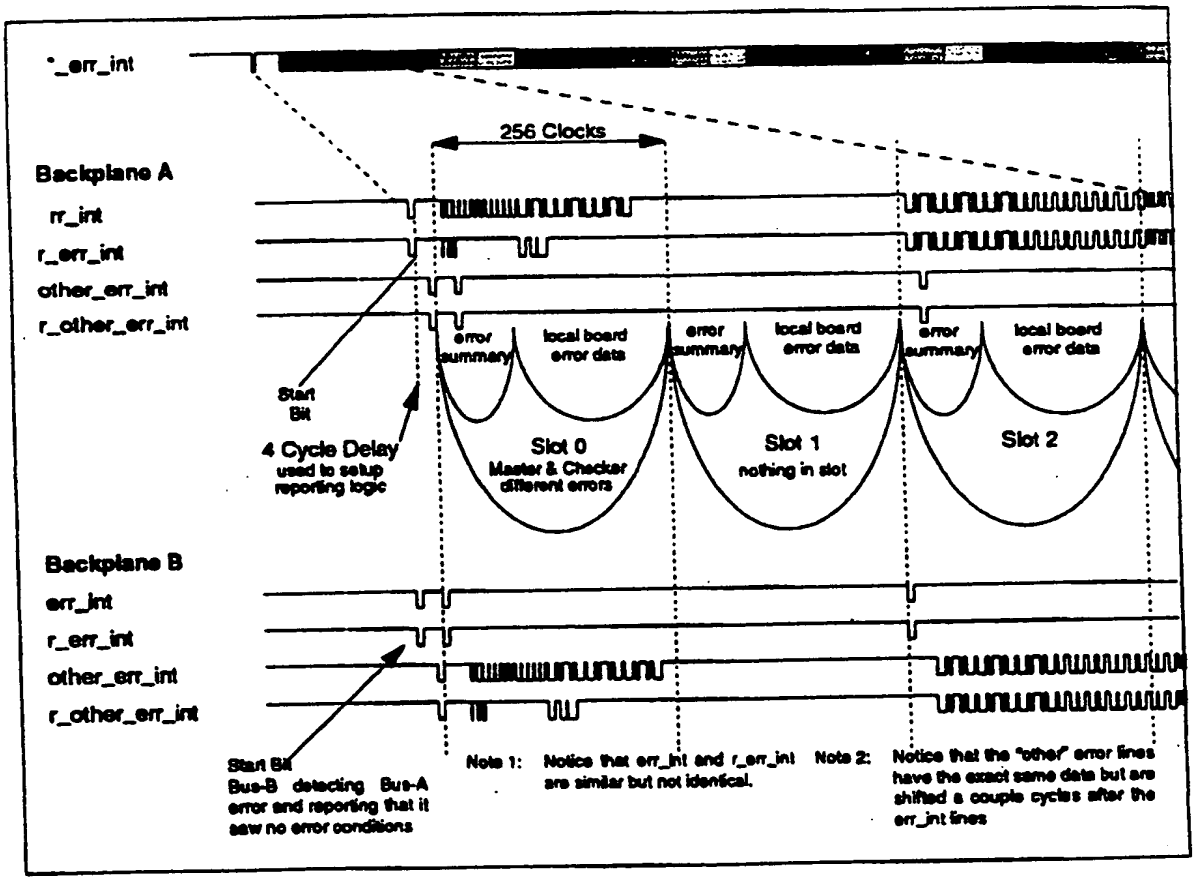
*_err_int
256 Clocks
Backplane A
rr_int
r_err_int
other_err_int
r_other_err_int
error summary
local board error data
error summary
local board error data
error summary
local board error data
Start Bit
4 Cycle Delay
used to setup reporting logic
Slot 0
Master & Checker different errors
Slot 1
nothing in slot
Slot 2
Backplane B
err_int
r_err_int
other_err_int
r_other_err_int
Start Bit
Bus-B detecting Bus-A error and reporting that it saw no error conditions
Note 1: Notice that err_int and r_err_int are similar but not identical.
Note 2: Notice that the "other" error lines have the exact same data but are shifted a couple cycles after the err_int lines

FIG. 10

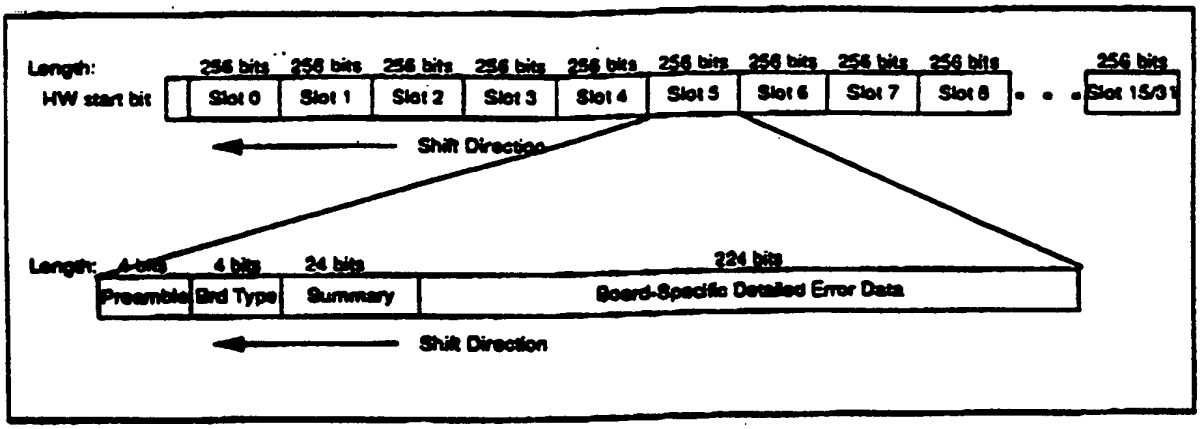
Length:
HW start bit
256 bits
Slot 0
Slot 1
Slot 2
Slot 3
Slot 4
Slot 5
Slot 6
Slot 7
Slot 8
Slot 15/31
Shift Direction
Length:
4 bits
24 bits
224 bits
Preamble
Brd Type
Summary
Board-Specific Detailed Error Data
Shift Direction

FIG. 11

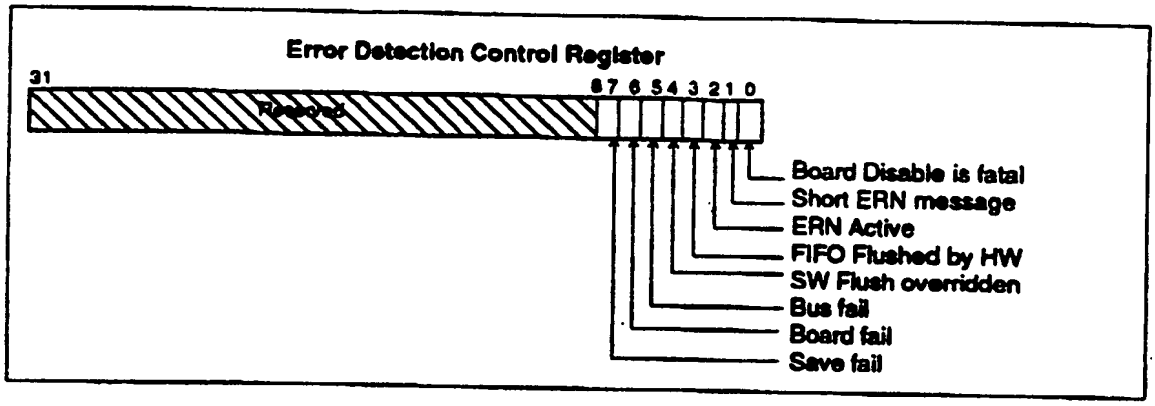
Error Detection Control Register
31
Reserved
8 7 6 5 4 3 2 1 0
Board Disable is fatal
Short ERN message
ERN Active
FIFO Flushed by HW
SW Flush overridden
Bus fail
Board fail
Save fail

FIG. 12

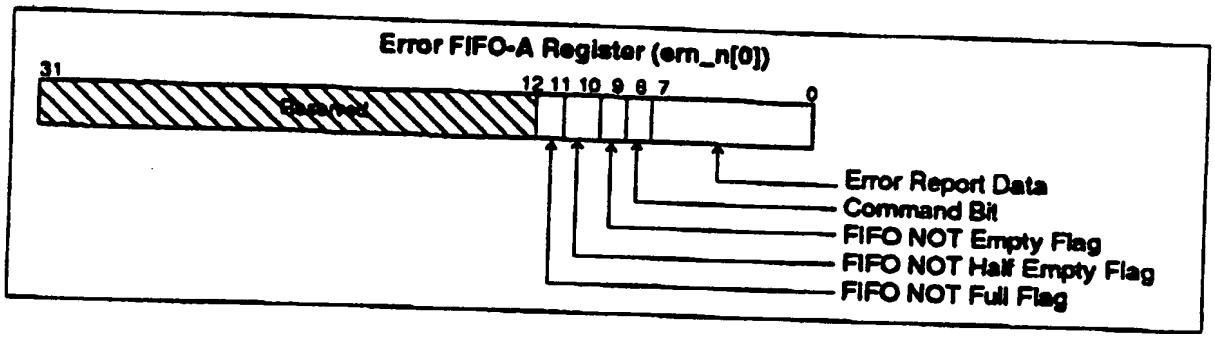
Error FIFO-A Register (ern_n[0])
31
12 11 10 9 8 7
0
Reserved
Error Report Data
Command Bit
FIFO NOT Empty Flag
FIFO NOT Half Empty Flag
FIFO NOT Full Flag

FIG. 13

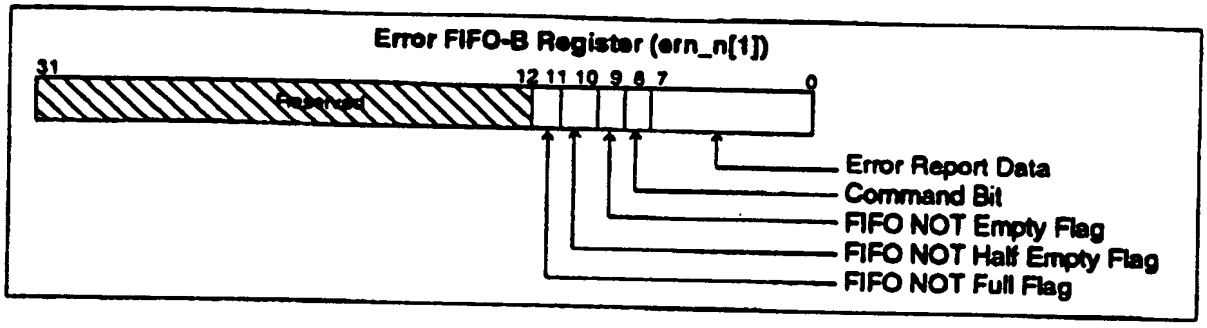
Error FIFO-B Register (ern_n[1])
31
12 11 10 9 8 7
0
Reserved
Error Report Data
Command Bit
FIFO NOT Empty Flag
FIFO NOT Half Empty Flag
FIFO NOT Full Flag

FIG. 14

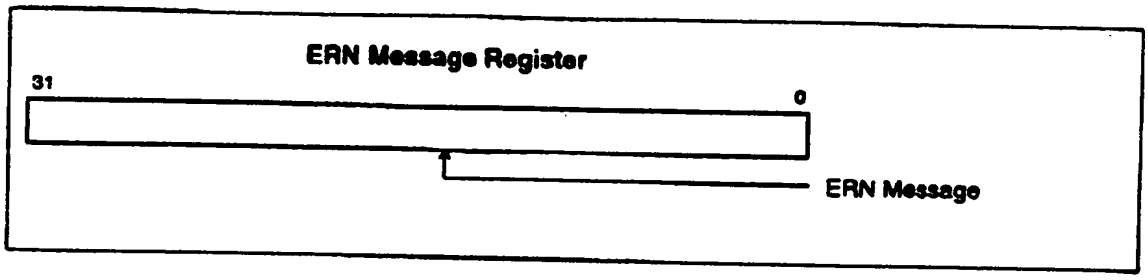

FIG. 15